INFORMATION DISCLOSURE CITATION FEB 24 2005 PATENT & TRADEMARK OFFICE PTO-1449	Complete If Known	
	Application Number	10/662,204
	Filing Date	September 12, 2003
	First Named Inventor	Nguyen et al.
	Art Unit	2819
	Examiner Name	Cho, James Hyonchol
Sheet 1 of 2	Attorney Docket Number	60809-0127-US

U.S. PATENT DOCUMENTS

Examiner Initials	Document Number Number - Kind Code[1]	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Filing Date if Appropriate
JC	5,182,467	01/1993	Taylor et al.	327	175	
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Examiner Initials	Foreign Patent Document Country Code[2] - Number[3] - Kind Code[4] (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Class	Subclass	Translation Yes	Translation No
JC	EP 0 463 316 A1	01/02/1992		H04L	12/40	✓	
JC	EP 0 482 392 A2	04/29/1992		H04L	25/08	✓	
JC	JP 58-54412 (A)	03/31/1983		G05F1	56	abstract only	

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS

Examiner Initials	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published
	Allen, Arnold O., "Probability, Statistics, and Queuing Theory with Computer Science Applications", 2nd Edition, CH 7, pp 450, 458-459
JC	Chappell, Terri I. et al., "A 2ns Cycle, 4ns Access 512 kb CMOS ECL SRAM", *IEEE International Solid State Circuits Conference*, 1991, pp 50-51 No month
JC	Donnelly, Kevin S. et al., "A 660 MB/s Interface Megacell Portable Circuit in 0.3 μm-0.7 μm CMOS ASIC", *IEEE Journal of Solid State Circuits*, 31(12):1995-2003 (1996) No month

Transcript count of No Date

Examiner Signature	James Cho	Date Considered	8/2/05

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JC	Pilo, Harold et al., "A 300 MHz 3.3V 1 Mb SRAM Fabricated in a 0.5 μm CMOS Process", *IEEE International Solid State Circuits Conference*, pp. 148-149 (1996) No month
	Schumacher, Hans-Jürgen et al., "CMOS Subnanosecond True-ECL Output Buffer", *IEEE Journal of Solid-State Circuits*", 25(1):150-154 (1990) No month
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	Yang, Tsen-Shau et al., "A 4-ns 4Kx1-bit Two-Port BiCMOS SRAM", *IEEE Journal of D-State Circuits*", 23:(5):1030-1040 (1988) No month
	EIA/JDEC, JC-42.3 Committee on RAM Memories, Minutes of Meeting 63, July 21, 1992, Denver, CO.
JC	EIA/JDEC, JC-42.3 Committee on RAM Memories, Minutes of Meeting 64, Sept. 16-17, 1992, Crystal City, VA.

Examiner Signature	James Cho	Date Considered	8/2/05

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